AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

Please replace paragraphs [001] - [005], [041], [049], [077], [078], [083], [090], [091], [096], [104], [109], [110], [114], and [116] with the following paragraphs:

[001] U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, is hereby incorporated by reference.

[002] U.S. Patent Application Serial No. 10/035,589, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating-Point Computation with Detection and Representation of Inexact Computations Without Flags or Traps," assigned to the assignee of the present application, is hereby incorporated by reference.

[003] U.S. Patent Application Serial No. 10/035,595, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Adder With Embedded Status Information," assigned to the assignee of the present application, is hereby incorporated by reference.

[004] U.S. Patent Application Serial No. 10/035,580, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Multiplier With Embedded Status Information," assigned to the assignee of the present application, is hereby incorporated by reference.

[005] U.S. Patent Application Serial No. 10/035,647, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Divider With Embedded Status Information," assigned to the assignee of the present application, is hereby incorporated by reference.

[041] When carrying out a floating point operation involving extended precision exponents, the control module 110 multiplies the product of the factors of the numerator, $(A_1)*(A_2)*(A_3)*\cdots*(A_M)$, without causing an underflow or overflow, by grouping the factors into a number of groups and then using scaling unit 120 to scale and multiply the factor in each group. The control module 110 groups the factors of the numerator so that an overflow may not occur when the scaled factors of a group are multiplied together. Accordingly, the control module 110 may group the factors into M/M_1 groups wherein each group may comprise M_1 factors or less. If a factor, A_n, is the sum of two floating point values (e.g., $a_n + b_n$), the sum is generated prior to being processed by scaling unit 120. The sum may be generated using an adder unit according to U.S. Patent Application Serial No. 10/035,595, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Adder With Embedded Status Information," assigned to the assignee of the present application, for example.

[049] The result of equation (2) may be computed by dividing the final product of the numerator, $PRODUCT_{NUM}$, by the final product of the denominator, $PRODUCT_{DEN}$, to obtain a scaled quotient, which value will be in a floating point representation. The scaled quotient may be generated using a divider unit according to U.S. Patent Application Serial No. 10/035,647, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Divider With Embedded Status Information,"

assigned to the assignee of the present application, for example. The value of $PRODUCT_{NUM}/PRODUCT_{DEN}$ may be greater than one-half and less than two. The final scale factor of the denominator, SF_{DEN}, is subtracted from the final scale factor of the numerator, SF_{NUM}, to obtain a quotient scale factor, which may be in an integer representation. The final result, Q, may be generated by adjusting the value of the exponent of the scaled quotient by an amount relating to the quotient scale factor, as specified by the SCALB function in the appendix to IEEE Std. 754. Specifically, the final result Q may correspond to $SCALB(PRODUCT_{NUM}/PRODUCT_{DEN}, SF_{NUM} - SF_{DEN})$. This is notably accomplished without having to resort to traps to catch overflow and underflow situations.

[070] The extended exponent floating point unit 100 may receive operands or generate results having formats according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application. Fig. 13 depicts seven exemplary formats as disclosed U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, including a zero format 1310, an underflow format 1320, a denormalized format 1330, a normalized non-zero format 1340, an overflow format 1350, an infinity format 1360, and a not-a-number (NaN) format 1370.

[077] In addition, in one embodiment, a value in the other formats may be indicated as being inexact according to U.S. Patent Application Serial No. 10/035,589,

filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating-Point Computation with Detection and Representation of Inexact Computations Without Flags or Traps."

[078] Fig. 3 illustrates an exemplary embodiment of the scaling unit 120. In general, the scaling unit 120 may comprise operand buffers 300A and 300B, an operand analysis circuit 310, a processing circuit 320, and a result generator 330. The operand buffer 300A may receive a floating point operand, which corresponds to operand A discussed above. The operand buffer 300B may receive a floating point operand, which corresponds to operand B discussed above. The floating point operand 300A, 300B may be in a floating point format according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, U.S. Patent No. 6,131,106, or IEEE Std. 754.

[083] Fig. 4 illustrates an exemplary embodiment of a scaling unit 120a that may be used when the floating point operand stored in the operand buffer 300B may be in a format according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application. The scaling unit 120a may comprise operand buffers 300A and 300B an operand analysis circuit 310a, a processing circuit 320a, and a result generator 330a.

[090] The result generator 330a may be in the form of a floating point multiplier unit as disclosed in U.S. Patent Application Serial No. 10/035,580, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Multiplier With Embedded Status Information," assigned to the assignee of the present application.

[091] Fig. 5 illustrates an exemplary embodiment of a scaling unit 120b that may be used when the floating point operand stored in the operand buffer 300B may be in a format according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, but, instead of the denormalized format 1330, the operand may be in a delimited format according to U.S. Patent No. 6,131,106.

[096] Turning to Fig. 8, exemplary running sum unit 130 may comprise operand buffers 800A, 800B, an operand analysis circuit 810, a processing circuit 820, and a result generator 830. The operand buffer 800A may receive an integer operand, which corresponds to operand J discussed above. The operand buffer 800B may receive a floating point operand, which corresponds to operand F discussed above. The floating point operand may be in a floating point format according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, U.S. Patent No. 6,131,106, or IEEE Std. 754.

[104] Fig. 9 illustrates an exemplary embodiment of a running sum unit 130a that may be used when the floating point operand stored in the operand buffer 800B

may be in a format according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application. The running sum unit 130a may comprise an operand analysis circuit 810a, a processing circuit 820a, and a result generator 830a.

[109] The result generator 830a may comprise a sign extender circuit 64 and a subtraction circuit 65. The sign extender circuit 64 receives the signals provided by the processing circuit 820a and performs a sign extension operation. The subtraction circuit 65 may receive the signals representing the integer operand in operand buffer 800A and the signals generated by the sign extender circuit 64, both in two's complement form, and generate signals representative of their difference. The result is coupled to result bus 35.

[110] Fig. 10 illustrates an exemplary embodiment of a running sum unit 130b that may be used when the floating point operand stored in the operand buffer 800B may be in a format according to U.S. Patent Application Serial No. 10//035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, but, instead of the denormalized format 1330, the operand may be in a delimited format according to U.S. Patent No. 6,131,106. The running sum unit 130b is identical to the running sum unit 130a described above, except that running sum unit 130b includes a count trailing zeros circuit 161 instead of a count leading zeros circuit 61. More specifically, the count trailing zeros circuit 161 generates output signals representing the number n, where n equals the number of bits equal to

zero to the right of the delimiter flag. Otherwise, the running sum unit 130b operates in the same manner as running sum unit 130a.

[114] Further, the above description of the extended exponent floating point unit 100 has been described with reference to operands according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, U.S. Patent No. 6,131,106, and IEEE Std. 754. However, those skilled in the art will appreciate that the extended exponent floating point unit 100 may be adapted to receive a floating point operand having a different format. Adapting the extended exponent floating point unit 100 to receive a floating point operand having a different format will be obvious to those of ordinary skill in the art.

[116] Finally, the scaling unit and the running sum unit may be included as functional units of the floating point units disclosed in U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application.